AN ADAPTIVE HYBRID ARQ SCHEME WITH CONCATENATED FEC CODES FOR WIRELESS ATM

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ABSTRACT

This paper describes the design and performance of a hybrid ARQ scheme with the concatenated FEC for wireless ATM networks. The wireless channel is characterized by burstier error patterns, and a higher and time-varying error rate when compared with the fiber-based network for which ATM was designed. The purpose of the hybrid ARQ scheme with the concatenated FEC is to provide a capability to dynamically support survivable ATM-based communications on a wireless channel by using a combination of ARQ and FEC schemes. The key ideas of the proposed hybrid scheme are the adaptation of the code rate to the channel conditions using incremental redundancy and the increase of the starting code rate as high as possible with the concatenated FEC to maximize the throughput efficiency. The simulation results show that our proposed scheme outperforms other hybrid ARQ schemes for all SNR values.

1. INTRODUCTION

In recent years, wireless ATM has emerged as a solution for mobile multimedia by supporting ATM-based transport in a seamless manner [12]. The attempt of ATM over wireless links immediately identifies a fundamental difference in the way that ATM will be used. That is, ATM will be subject to transmission links that are unreliable radio links. Because of the fading effects and interference, the wireless link is characterized by burstier error patterns, and a higher and time-varying error rate when compared with the fiber-based network for which ATM was designed. As a result, such difference leads to error control schemes to insulate the ATM network layer from wireless channel impairments.

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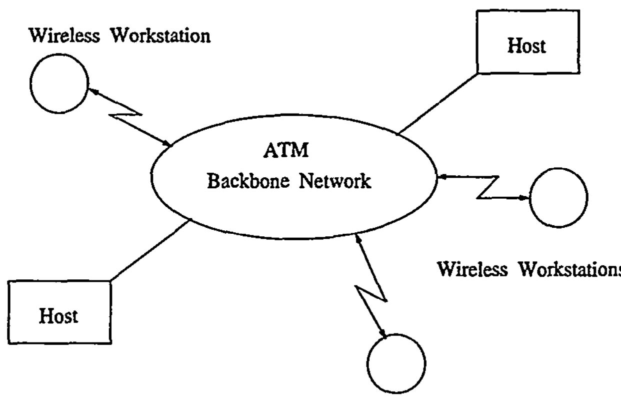

Figure 1: System Architecture for Wireless ATM

There are two basic categories of error control schemes: ARQ (Automatic Repeat Request) and FEC (Forward Error Correction) schemes. ARQ schemes provide high reliability at good and moderate channel qualities. However, if the channel error rate is high like in a wireless channel, the throughput performance drops rapidly due to the increased frequency of retransmission. In order to counter this effect, hybrid ARQ schemes are used by combining FEC with ARQ schemes. In general, hybrid ARQ schemes are classified into type I and type II schemes. In type I hybrid scheme, each packet is encoded for both error detection and error correction. At the receiver, the FEC portion first attempts to correct the frequent error patterns. If an uncorrectable error pattern is detected, then the receiver requests a retransmission using ARQ.

Error statistics on the wireless channel are time-varying. Efficient error control for a time-varying channel can be realized with an adaptive coding scheme. The type II hybrid scheme is an adaptive coding scheme with two code rates. When the channel condition is good, the high code rate is used for error detection. In response to the retransmission request, redundant parity bits are sent to the receiver and combined with the previous error packet to produce the low code rate for error correction. This scheme is generalized with code combining to offer a large number of code rates instead of two as in the type II hybrid case.

We envision a system architecture for wireless ATM which has a backbone network consisting of ATM switches as shown in Figure 1. Wireless workstations (mobile or fixed) communicate with stationary hosts through the backbone network where some portions could be wireless. Stationary hosts are connected to the backbone network by wired lines. In this architecture, a wireless link refers to either a link between a wireless workstation and an ATM switch or a link between ATM switches.

As an operational example, the following scenario will apply. User A is the originator of the request for information, residing on a workstation with wireless access to the ATM switch. User B is the source of the information, residing in a stationary host such as a command center. To perform the mission, user A communicates with user B by using a set of multimedia services.

In this paper, we propose an adaptive hybrid ARQ scheme using concatenated FEC codes for wireless ATM. In the next section we discuss the ATM HEC performance, followed by an analysis of the concatenated FEC approach for wireless ATM in Section 3. In Section 4 we describe the proposed hybrid scheme which is adaptive to channel conditions using incremental redundancy. In Section 5 we present throughput efficiency of the proposed scheme and the simulation results over a wireless channel model. Finally we conclude the paper by highlighting our contribution.

2. ATM HEC PERFORMANCE

The ATM cell consists of a 5-byte header and a 48-byte information payload field. The last octet of the header field is referred to as HEC (Header Error Control), calculated from the other four header octets. The HEC is used for two purposes: 1) protecting the ATM cell header to minimize misrouting and 2) identifying cell boundaries (CD: Cell Delineation).

The 8-bit HEC field is realized with a Cyclic Redundancy Check (CRC)-8 scheme. The (40,32) CRC code is derived from a (127,119) systematic cyclic code by shortening the code by 87 bits. Since shortening decreases the code rate, shortened codes have error detection and correction capabilities that are at least as good as those of the original code. The HEC's generator polynomial is given by,

$$g(x) = x^8+x^2+x+1 = (x+1)(x^7+x^6+x^5+x^4+x^3+x^2+1) \quad (1)$$

where the second term is a primitive polynomial.

HEC operates in two modes: correction mode and detection mode. In the ATM Forum [2], the detection mode is mandatory while the correction mode is optional. When in the correction mode, a single-bit error can be corrected and cells with multiple-bit errors are discarded. Any detected error triggers a transition to the detection mode. When in the detection mode, all cells detected in errors are discarded.

Let $r(x)$ be the received polynomial. The remainder of $r(x)/g(x)$ is called syndrome. There exist 256 (=2^8) syndrome patterns in which only one pattern indicates no error (syndrome=0), 40 patterns single-bit errors, and the remaining 215 patterns multiple-bit errors. In the correction mode, if multiple-bit errors create one of 41 syndrome patterns corresponding to no error or a single-bit error, it cannot be detected and thus the error detection coverage is 0.84 (1 - 41/256). Similarly, in the detection mode the error detection coverage is 0.9961 (1 - 1/256). HEC is capable of correcting single errors and detecting all double and a large fraction of multiple-bit errors. Since the generator polynomial $g(x)$ contains $(x+1)$ as a factor, it can also detect all odd number of bit errors. With the generator polynomial of degree 8, the burst-error detecting performance of HEC is as follows:

- Detects all single bursts of length 8 or less.
- Detects 99.22% of all error bursts of length 9.
- Detects 99.61% of all error bursts of length 10 or more.

Since fiber-based links have rare and independent error patterns with a mix of single-bit errors and relatively large burst errors, the HEC will show good performance in this case by correcting single-bit errors and detecting burst errors. However, with wireless links the HEC mechanism will encounter severe performance degradation due to their much higher and correlated error characteristics.

In the following, we discuss the ATM HEC performance over a wireless channel. For BPSK (Binary Phase Shift Keying) or QPSK (Quaternary Phase Shift Keying) with coherent detection on an AWGN (Additive White Gaussian Noise) Rayleigh fading channel, the probability of bit error is given by [11],

$$P_b = \frac{1}{2}\left(1 - \sqrt{\frac{\gamma_b}{1+\gamma_b}}\right) \quad (2)$$

where γ_b is the average signal-to-noise ratio per bit. Ideal interleaving produces independent bit errors. Without using the HEC function, the cell loss probability (CLR) results from the ATM cell header in error:

$$CLR_{noHEC} = 1 - (1 - P_b)^{32} \quad (3)$$

where 32 is the ATM cell header size in bits without HEC.

When the HEC function is used in the correction/detection mode, the cell loss probability (CLR) is given by,

$$\begin{aligned} CLR_{HEC} &= P_c P_m + P_d(P_1 + P_m) \\ &= 1 - P_0 - P_0 P_1 \end{aligned} \quad (4)$$

where,
$P_c = P_0$ is the probability in the correction mode
$P_d = (1 - P_c)$ is the probability in the detection mode
$P_0 = (1 - P_{b'})^{40}$ is the probability of no error in an ATM cell header
$P_1 = 40(1 - P_{b'})^{39} P_{b'}$ is the probability of a single-bit error in an ATM cell header
$P_m = 1 - P_0 - P_1$ is the probability of multiple-bit errors in an ATM cell header.
$P_{b'}$ is the modified probability of bit error from Eq. (2):

$$P_{b'} = \frac{1}{2}\left(1 - \sqrt{\frac{\frac{32}{40}\gamma_b}{1+\frac{32}{40}\gamma_b}}\right) \quad (5)$$

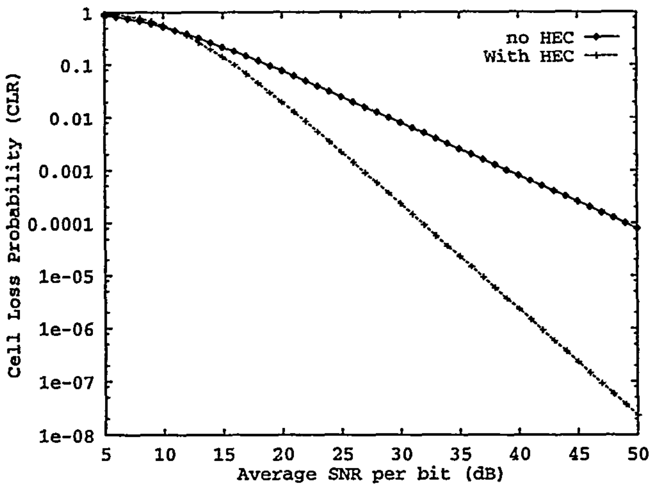

Figure 2: ATM HEC Performance on AWGN Rayleigh Fading Channel

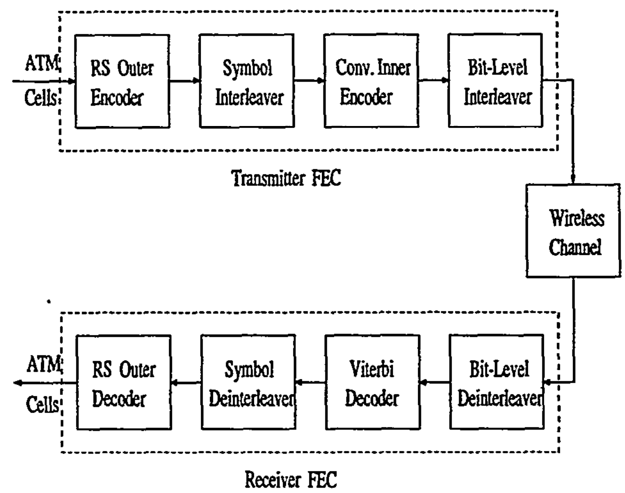

Figure 3: Concatenated FEC Scheme for Wireless ATM

where 32/40 is the code rate of the (40,32) CRC code for the ATM header. As shown in Figure 2, adding HEC provides a larger coding gain on a Rayleigh fading channel with the increasing SNR (Signal-to-Noise Ratio). However, since HEC is not enough for wireless ATM and furthermore there is also a high probability of corrupted ATM payloads, FEC must be utilized to protect the ATM payload and to achieve performance gain desired for wireless ATM.

The ATM cell delineation (CD) method is based on the HEC check. If a certain number of consecutive correct HECs are found, the receiver goes to the SYNC state. While in the SYNC state, synchronization is lost only if a certain number of consecutive incorrect HECs occur. In fiber-based links, the receiver is in the SYNC state most of the time. However, in wireless links the receiver may easily lose synchronization, which may lead to severe performance degradation in the CD mechanism. Likewise, FEC schemes are required to provide considerable protection for the ATM header.

3. THE CONCATENATED FEC APPROACH FOR WIRELESS ATM

In wireless ATM, channel errors will be typically beyond the error correcting capability of the ATM HEC (Header Error Control), making it necessary for more powerful FEC schemes. The performance of FEC schemes can vary depending on various factors, such as code rate, channel model, and so on. However, there is a fundamental limit on performance that can be achieved. This is also true for wireless ATM.

Shannon proved that it is possible to send data over even a noisy channel with an arbitrarily low error rate, as long as the data rate is less than the channel capacity [13]. The basic idea behind FEC is to correct channel errors at the expense of increased bandwidth by adding redundancy. Given that the data rate is equal to the channel capacity, the fundamental limit on the SNR per bit (E_b/N_0) is obtained as the channel bandwidth approaches infinity, which is called the Shannon limit [13].

$$\frac{E_b}{N_0}(Shannon\ Limit) = -1.6dB \tag{6}$$

Basically, there are three FEC approaches that can be used for wireless ATM.

- Convolutional coding with Viterbi decoding
- Concatenated FEC scheme
- Turbo coding

Convolutional coding provides substantial coding gain with respect to an uncoded system. However, the gain is not sufficient. Moreover, the Viterbi decoder errors are typically beyond the HEC's correction capability due to the burstiness.

As shown in Figure 3, the concatenated FEC scheme uses a convolutional inner code and an RS (Reed-Solomon) outer code with interleaving [4, 14]. The RS code is used as an outer code to correct burst errors out of the Viterbi decoder and offers as much performance gain as desired for wireless ATM.

Recently, Turbo coding has been introduced in [3], based on a parallel concatenation of recursive convolutional codes and an iterative decoding process. The performance has been shown to be almost equivalent to that of the concatenated coding scheme.

In this section, we analyze the performance of the concatenated scheme on an AWGN Rayleigh fading channel, and then compare with other FEC schemes such as convolutional coding and Turbo coding under the same conditions. In particular, a rate-1/2, constraint-length 7 convolutional code with QPSK modulation is used as an inner code, since it is an industry standard in cellular radio systems. Since the performance of Viterbi decoding deteriorates in presence of burst errors, ideal interleaving is assumed to spread burst errors resulted from the wireless channel. The probability of bit error at the Viterbi decoder output, $P_{b,Vit}$, can be derived by using the transfer function $T()$ of convolutional codes and the union bound [5],

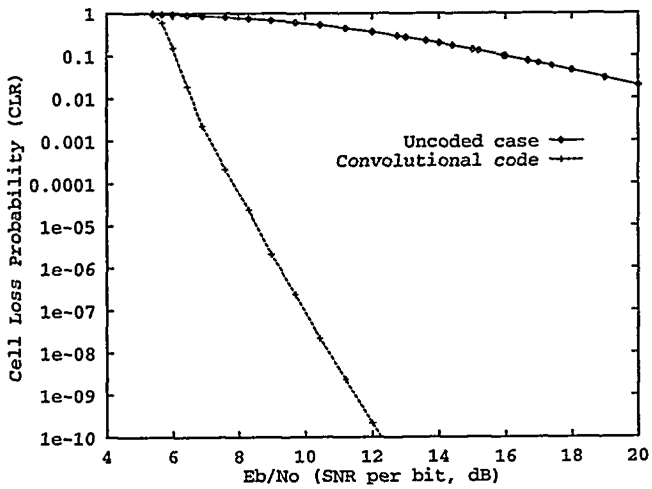

Figure 4: ATM HEC CLR for Rate-1/2, Constraint-length 7 Convolutional Coding on AWGN Rayleigh Fading Channel

$$P_{b,Vit} \leq \frac{1}{2} \left. \frac{\partial T(D_1, D_2, I)}{\partial I} \right|_{I=1} \tag{7}$$

where

$$D_1 = \frac{1}{1 + E_b/2N_0} \quad and \quad D_2 = \frac{1}{1 + E_b/N_0}$$

If this convolutional coding scheme is used below the ATM layer, then the resulting probability of bit error at the Viterbi decoder output, $P_{b,Vit}$, is the input probability of bit error to the ATM HEC function. Assuming that ideal interleaving randomizes error bursts from the Viterbi decoder, the resulting cell loss probability (CLR) as calculated by Eq. (4) is shown in Figure 4. For comparison, the uncoded case for the ATM HEC only is also shown in Figure 4. It is obvious that the convolutional codes with Viterbi decoding provide considerable coding gain relative to the uncoded case.

However, their performance is still not sufficient for wireless ATM. When the Viterbi decoder suffers a decoding error, the resulting codeword usually differs from the transmitted word by a few consecutive trellis branches. As a result, although the input to the Viterbi decoder is corrupted by random noise, the output of the decoder tends to have burst errors. This burst will typically be beyond the error correcting capability of HEC, causing a cell loss. Hence, the RS code with its inherent burst-error correcting capability is used to deal with burst errors out of the Viterbi decoder.

Since the constraint length is chosen to be 7 for convolutional coding, the most frequently occurring error bursts at the output of the Viterbi decoder will have length 7 or 8. Thus, 8-bit symbols are chosen for the RS code to handle these burst errors with a single RS symbol. The RS codeword takes the form of (n, k) over GF(2^8), where n is the number of code symbols and k is the number of information symbols. Since the minimum distance of this code is $n - k + 1$, it can correct i symbol errors and j symbol erasures at the same time as long as $(2i+j) \leq (n-k)$ is satisfied. The word error rate for a codeword of n symbols at the output of the RS decoder that is capable of correcting up to t symbol errors can be written as:

$$P_w = \sum_{2i+j>2t}^{i+j=n} \binom{n}{i,j} e^i s^j (1-e-s)^{n-i-j}, \; i,j \geq 0,1,2,\ldots \tag{8}$$

where e denotes the symbol error rate and s the symbol erasure rate before the RS decoder. For the concatenated coding scheme, the RS decoder processes the output stream of the Viterbi decoder. In this case, there are no symbol erasures ($s = 0$) and further the symbol error rate e at the input of the RS decoder is the same as the symbol error rate at the Viterbi decoder output, $P_{s,Vit}$. With ideal symbol interleaving between the Viterbi decoder and the RS decoder, Eq. (8) can be simplified to:

$$P_w = \sum_{i=t+1}^{n} \binom{n}{i} P_{s,Vit}^i (1 - P_{s,Vit})^{n-i} \tag{9}$$

When i (more than t) symbol errors occur, the RS decoder cannot correct them due to a decoder failure. Therefore, the symbol error rate after the RS decoder can be estimated by noting that i out of n symbols in an RS codeword will be delivered in error on a decoder failure. Furthermore, if about half of 8 bits in an errored RS symbol are assumed to be in error, then the probability of bit error at the RS decoder output is approximated as:

$$P_{b,RS} \approx \frac{1}{2} \sum_{i=t+1}^{n} \frac{i}{n} \binom{n}{i} P_{s,Vit}^i (1 - P_{s,Vit})^{n-i} \tag{10}$$

Since one RS symbol consists of 8 bits from the Viterbi decoder, the symbol error rate at the Viterbi decoder output, $P_{s,Vit}$, can be bounded as,

$$P_{s,Vit} < 8P_{b,Vit} \tag{11}$$

The symbol errors at the input of the RS decoder are assumed to be independent by using a symbol interleaver between two decoders, assuring that a given error burst from the Viterbi decoder affects no more than one symbol in an RS codeword. The evaluated results from Eq. (10) are presented in Figure 5 for the concatenated code of a rate-1/2, constraint-length 7 convolutional inner code and an $(n, 53)$ RS outer code for various error correcting capabilities (t = 2, 3, 4, 5, 8 symbols) on an AWGN Rayleigh fading channel with QPSK modulation. For comparison, the convolutional code alone case (t = 0) with the rate-1/2 and constraint-length 7 is also shown in Figure 5. The information size of the RS code is chosen to be 53 symbols, which corresponds to one ATM cell. The results show that the more error-correcting capability, the steeper performance curve with more coding gain, and consequently the concatenated coding scheme can offer sufficient error performance for wireless ATM. For example, with an 8-correcting RS code the coding gain is about 10.4 dB at the bit error rate of 10^{-10}

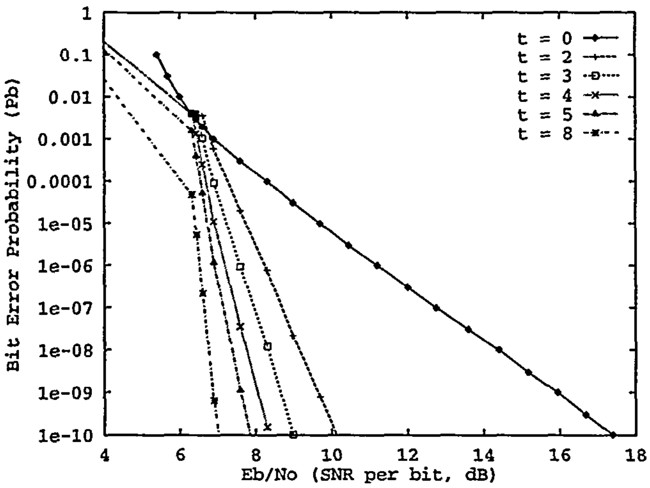

Figure 5: BER Performance of the Concatenated Scheme on AWGN Rayleigh Fading Channel

compared to the convolutional code alone case (t = 0) and the overall code rate is 0.384 (i.e., $1/2 * \frac{53}{53+16}$).

In [6], Turbo coding can provide equivalent performance to the concatenated scheme under the same conditions. However, Turbo coding often introduces a long coding delay due to the large interleaver and excessive computational complexity in the iterative decoding. This long delay hinders Turbo coding from being readily applied to real-time communication systems. Moreover, since it is not proven in the commercial market today, Turbo coding will be considered as a future work. Based on the performance evaluation, the concatenated scheme has been selected as our FEC approach for wireless ATM.

4. THE ADAPTIVE HYBRID ARQ SCHEME WITH CONCATENATED FEC

Since convolutional codes are used as an inner code in the concatenated FEC scheme as shown in Figure 3, incremental redundancy can easily be implemented by imposing the rate compatibility condition on the convolutional codes. For wireless ATM, we propose an efficient hybrid ARQ scheme in order to adapt to channel conditions based on the incremental redundancy.

4.1. The Rate Compatible Convolutional Codes

A family of convolutional codes are defined as *rate compatible* [8] if all the code bits of the higher rate codes are included in the lower rate codes. These rate compatible convolutional (RCC) codes are obtained from an original rate-1/2 convolutional code by using "rate tables" for puncturing or repetition. The rate table indicates which of the bits are to be punctured or repeated prior to transmission for each code rate. Each entry of a rate table is zero or a positive integer. A zero denotes puncturing and a positive integer denotes the number of repetitions of the corresponding code bit. These tables operate on each group periodically with a period of P to generate a family of RCC codes with code rates:

$$R = \frac{P}{P+i} \qquad i = 0, 1, 2 \ldots \quad (12)$$

Each table consists of two rows and P columns. The highest rate RCC code (i.e., P/P) is obtained from a rate-1/2 convolutional code by puncturing P bits from each group of 2P code bits according to the rate table. For example, the rate table A_0 of a rate-8/8 punctured convolutional code, obtained from a rate-1/2 code with constraint-length 7 is given by [15],

$$A_0 = \begin{bmatrix} 1 & 1 & 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix} \quad (13)$$

where P is chosen to be 8 bits for byte processing.

Starting with the rate P/P punctured code, RCC codes of lower rates can be obtained by simply inserting bits at the punctured bit positions. When all P bits are inserted, the original rate-1/2 code is recovered. As an example, an RCC code of rate-8/12 can be obtained by adding four more bits to the A_0 table above according to the following rate table [8]:

$$A_1 = \begin{bmatrix} 1 & 1 & 1 & 1 & 0 & 1 & 0 & 1 \\ 1 & 0 & 1 & 0 & 1 & 1 & 1 & 1 \end{bmatrix} \quad (14)$$

Similarly, RCC codes of rates lower than 1/2 can be obtained by repeating some bits specified by the rate table, depending on a given code rate. There is no limit to the lowest achievable code rate with RCC codes. In summary, RCC codes can provide an efficient way of implementing incremental redundancy using the same encoder/decoder. Moreover, these codes can also provide variable rate error protection through a large selection of code rates, particularly useful for multimedia applications with different QoS (Quality of Service) requirements.

4.2. The Hybrid ARQ Scheme

The proposed hybrid scheme is not to repeat information bits in response to the retransmission request, but transmit additional parity bits only using incremental redundancy of RCC codes until the combined code is powerful enough for error correction. The key idea to the scheme is to adapt the code rate to the channel conditions, maximizing the throughput efficiency. The starting code rate and the number of incremental redundancy bits are to be chosen according to the channel condition at that time. Since the concatenated FEC scheme is used here and RS codes have small overhead, RS codes will be included as much as possible, so as to reduce the large overhead of convolutional codes. As a result, when compared with the convolutional coding only case, the starting code rate of the concatenated FEC scheme increases at a given channel condition, leading to higher throughput.

The hybrid ARQ scheme with the concatenated FEC scheme is similar to the one proposed by Kallel [10]. Our own ARQ protocol is assumed here, which is based on the selective reject (SR-ARQ) protocol [1]. Let the window size

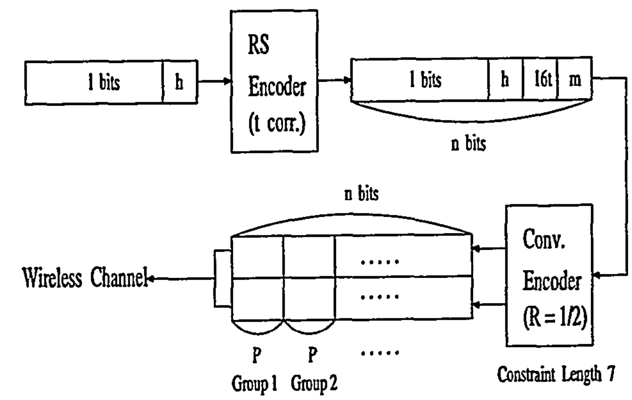

Figure 6: Encoding Scheme with Concatenated FEC

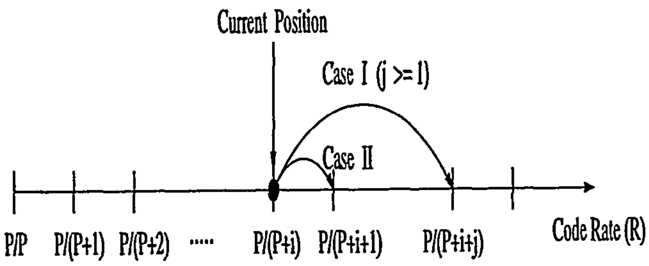

Figure 7: Adaptive Code Rate to the Channel Condition using Incremental Redundancy

be W and the receiver buffer size be sW, where s is a positive integer. As shown in Figure 6, to each l-bit information payload, h control bits are added per packet including traffic type and CRC bits, $16t$ bits from the RS outer encoder, and then m tail bits for trellis termination where m is the memory size of the convolutional encoder. The error correcting capability t of RS codes is determined such that the starting code rate R_0 of the convolutional encoder increases as much as possible under the current channel condition based on the performance curves as shown in Figure 5, maximizing the throughput efficiency. The sequence of n bits $(l+h+16t+m)$ is then encoded with the rate-1/2, constraint-length 7 convolutional encoder and transmitted using the following procedure. To begin with, let r_i be the number of incremental redundancy bits at Step i.

Step 0: Given the starting code rate $R_0 = P/(P+r_0), r_0 \geq 0$, the encoded sequence is transmitted according to the rule defined by the rate table of R_0 described in Section 4.1. At the receiver, the received sequence is decoded by the Viterbi decoder then the RS decoder, and checked with the CRC bits for error detection. If there is no error in the sequence, then the procedure stops. Otherwise, a retransmission request is sent to the transmitter and the procedure moves to Step 1.

Step i, $1 \leq i < s$: In response to the retransmission request, only incremental redundancy bits r_i are transmitted at this Step i using the rate table with the code rate $R_i = P/(P+r_0+\ldots+r_i), r_i \geq 1$. The size of r_i is determined based on the channel condition at this point. There are two cases to be considered. First, if the channel condition becomes worse compared to the previous channel condition, r_i will be chosen to adapt to the current channel condition as shown in the case I of Figure 7. On the other hand, if the channel condition is still the same or unusually becomes better, r_i will be set to the minimum incremental level, which is just one bit as shown in the case II of Figure 7. This is because adapting to the channel condition does not give any redundancy bits to transmit. At the receiver, the redundancy bits are combined with the previously received sequence for decoding by the Viterbi decoder and the RS decoder. The decoded sequence is checked with the CRC bits for error detection. If there is no error in the sequence, then the procedure stops. Otherwise, a retransmission request is sent to the transmitter and the procedure moves to Step $i+1$.

Step i, $i \geq s$: In response to the retransmission request, incremental redundancy bits r_s are transmitted using the rate table with the code rate $R_i = P/(P+r_0+\ldots+r_{s-1}+(i-s+1)r_s), r_s \geq 1$. Because of buffer overflow in the worst case, incremental redundancy bits are not increased any more and W packets are chosen to be discarded from the receive buffer, based on the priority of the packets. That is, packets on this incremental procedure have priority over other normal packets, or real-time traffic is loss-tolerant, etc. At the receiver, the redundancy bits are combined with the previously received sequence for decoding by the Viterbi decoder and the RS decoder. The decoded sequence is checked with the CRC bits for error detection. If there is no error in the sequence, then the procedure stops. Otherwise, a retransmission request is sent to the transmitter and the procedure moves to Step $i+1$.

5. PERFORMANCE EVALUATION

5.1. Throughput Analysis

The throughput is defined as the average number of actual information bits per transmitted channel bit. Let E_i be the decoding error event for each packet occurring together at the Viterbi decoder then the RS decoder at Step i. The expected value of transmitted channel bits E[N] per correctly accepted l-bit information payload is given by,

$$\begin{aligned} E[N] &= \frac{n}{R_0} + \frac{nr_1}{P}Pr(E_0) + \ldots + \frac{nr_{s-1}}{P}Pr(E_0,\ldots,E_{s-2}) \\ &+ \left(\frac{nr_s}{P} + nW\right)\cdot[Pr(E_0,\ldots,E_{s-1}) + Pr(E_0,\ldots,E_s) \\ &+ \ldots] \end{aligned} \tag{15}$$

where R_0 denotes the starting code rate, r_i the incremental redundancy bits at Step i, P the period of RCC codes, and W the window size.

$$n = l + h + 16t + m \tag{16}$$

where l denotes the information payload bits, h the packet control bits, t the error correcting capability in bytes of RS codes, and m the memory size of the convolutional encoder. The throughput η is then given by,

$$\eta = \frac{1}{E[N]} \cdot \frac{l}{n} \tag{17}$$

The exact evaluation of $Pr(E_0, E_1, \ldots)$ is difficult due to the statistical dependencies among error events. However, we can obtain a lower and an upper bound using the following inequalities [8]:

$$\prod_{j=0}^{i} Pr(E_j) \leq Pr(E_0, E_1, \ldots, E_i) \leq Pr(E_i) \qquad (18)$$

5.2. Simulation Results

In this section, the throughput of the proposed hybrid ARQ scheme is evaluated for a wireless channel model using an AWGN Rayleigh fading channel with binary FSK modulation. The decoding error event for each packet consists of two individual events, E_{Vit} and E_{RS}, at the Viterbi decoder and the RS decoder respectively. Since convolutional codes are used as an inner code and RS codes as an outer code in the concatenated FEC scheme, these two error events are sequential and dependent. At each procedure step, the probability of a decoding error $Pr(E_i)$ for a particular packet corresponds to the word error rate P_w at the output of the RS decoder from Eq. (9) described in Section 3. The only difference is that since FSK modulation is used here instead of QPSK for comparison with other typical ARQ schemes, the probability of bit error $P_{b,Vit}$ at the output of the Viterbi decoder is different.

Let β_d be the coefficients of the derivative of the convolutional code transfer function $T()$. Given the free distance d_{free,R_i} and β_{d,R_i} at the code rate R_i, the probability of bit error at the output of the Viterbi decoder with the code rate R_i used at Step i is given by [11],

$$P_{b,Vit}(R_i) < \frac{1}{n} \sum_{d=d_{free,R_i}}^{\infty} \beta_{d,R_i} P_d \qquad (19)$$

where n denotes the input sequence bits to the convolutional encoder and P_d the probability that a wrong path of weight d is selected. Let the average received SNR per bit γ_b. With soft decision, the probability of P_d is given by [11],

$$P_d = p^d \sum_{k=0}^{d-1} \binom{d-1+k}{k} (1-p)^k \qquad (20)$$

where $p = \frac{1}{2+R_0\gamma_b}$. From these equations, lower bounds on the throughput of the proposed ARQ hybrid scheme with the concatenated FEC can now be calculated.

In order to evaluate the throughput of the hybrid ARQ scheme for the concatenated FEC, the starting code rate R_0 should be considered first as shown in Eq. (15). Using Eq. (10) for the performance results of the concatenated FEC, we can compare with the convolutional code case in terms of the code rate. As shown in Figure 8, the concatenated FEC can increase the code rate by taking advantage of the small overhead of RS codes at a given channel condition. In fact, since the performance curve of the concatenated scheme is much steeper than that of the convolutional code, the higher the error performance the larger the difference of the code rate between two coding schemes. For example, a convolutional code with soft decision and perfect channel state information can achieve the BER performance of 10^{-9} with

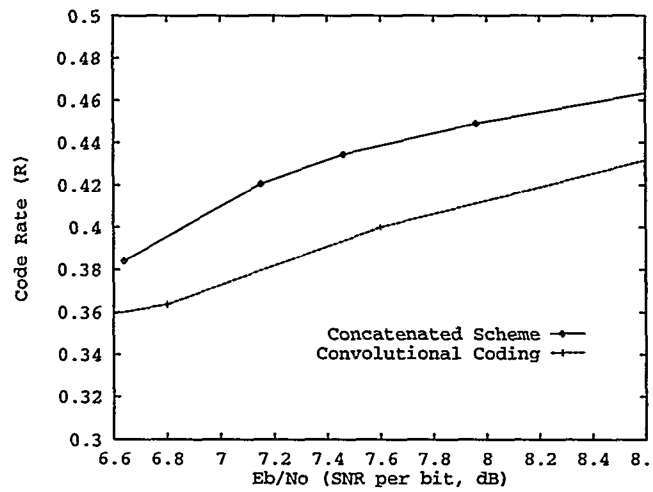

Figure 8: Comparison between Concatenated Scheme and Convolutional Coding at the BER 10^{-7} in terms of Code Rate

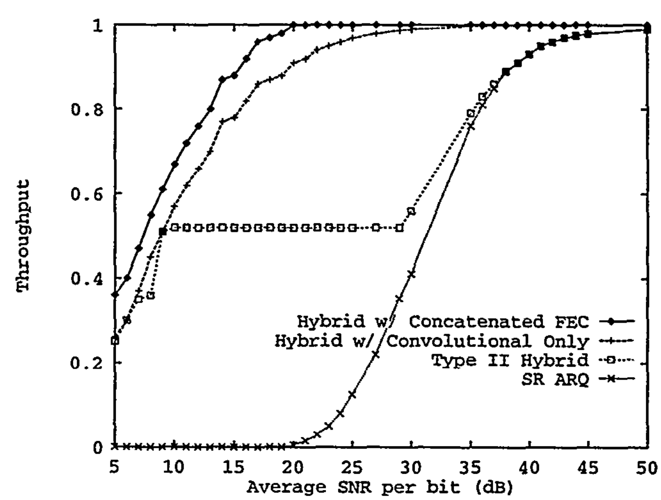

Figure 9: Throughput of Hybrid ARQ Scheme using Concatenated FEC on an AWGN Rayleigh Fading Channel

$E_b/N_0 = 7.6$ dB and code rate $= 1/3$ on an AWGN Rayleigh fading channel [7]. Instead, the concatenated scheme offers the same performance with the overall code rate of about 0.421, which is much better than that of the convolutional code case.

The lower bounds on the throughput of the proposed hybrid scheme with $P = 8, s = 1$, optimized over all values of R_0 and R_1 for $n = 500$ and $W = 10$, are presented in Figure 9. For comparison, the throughput curves for the hybrid ARQ scheme with convolutional codes [10], Type II hybrid ARQ scheme [9], and classical SR-ARQ [16] are also plotted in Figure 9. The results show that our proposed scheme outperforms other ARQ schemes for all SNR values. Moreover, the more error performance is required, the higher throughput is expected due to the difference of the starting code rate.

6. CONCLUSIONS

In this paper, we have discussed the design and performance of a hybrid ARQ scheme with the concatenated FEC for wireless ATM. The performance of a concatenated FEC scheme has been analyzed over an AWGN Rayleigh fading channel, showing that it can provide sufficient error performance for wireless ATM. The key ideas to the proposed hybrid scheme are to adapt the code rate to the channel conditions using incremental redundancy and to increase the starting code rate as much as possible with the concatenated FEC, maximizing the throughput efficiency. This strategy allows the system to be flexible and adaptive to channel conditions, especially suitable for a time-varying channel with high error rates such as a wireless channel. The simulation results show that our proposed scheme outperforms other ARQ schemes for all SNR values.

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